EXHIBIT 13

US006677776B2

(12) **United States Patent**
Doherty et al.

(10) **Patent No.: US 6,677,776 B2**
(45) **Date of Patent: *Jan. 13, 2004**

(54) **METHOD AND SYSTEM HAVING SWITCHING NETWORK FOR TESTING SEMICONDUCTOR COMPONENTS ON A SUBSTRATE**

(75) Inventors: **C. Patrick Doherty**, Boise, ID (US); **Salman Akram**, Boise, ID (US); **Jorge L. de Varona**, Boise, ID (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **10/223,826**

(22) Filed: **Aug. 20, 2002**

(65) **Prior Publication Data**

US 2002/0196047 A1 Dec. 26, 2002

Related U.S. Application Data

(63) Continuation-in-part of application No. 09/999,502, filed on Dec. 4, 2002, now Pat. No. 6,466,047, which is a division of application No. 09/675,072, filed on Sep. 28, 2000, now Pat. No. 6,433,574, which is a division of application No. 09/244,373, filed on Feb. 4, 1999, now Pat. No. 6,337,577, which is a continuation-in-part of application No. 09/075,691, filed on May 11, 1998, now Pat. No. 6,246,250.

(51) **Int. Cl.**[7] **G01R 31/26**
(52) **U.S. Cl.** **324/765**; 324/158.1
(58) **Field of Search** 324/765, 754, 324/158.1, 755, 758; 438/6, 14, 17

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,806,801	A	4/1974	Bove
4,027,935	A	6/1977	Byrnes et al.
4,585,991	A	4/1986	Reid et al.
4,891,585	A	1/1990	Janko et al.
4,906,920	A	3/1990	Huff et al.
4,918,383	A	4/1990	Huff et al.
4,954,458	A	9/1990	Reid
5,042,148	A	8/1991	Tada et al.
5,053,700	A	10/1991	Parrish
5,055,780	A	10/1991	Takagi et al.
5,070,297	A	12/1991	Kwon et al.
5,103,557	A	4/1992	Leedy
5,124,639	A	6/1992	Carlin et al.
5,172,050	A	12/1992	Swapp
5,177,439	A	1/1993	Liu et al.
5,180,977	A	1/1993	Huff
5,196,726	A	3/1993	Nishiguichi et al.
5,225,037	A	7/1993	Elder et al.
5,264,787	A	11/1993	Woith et al.
5,323,107	A	6/1994	D'Souza
5,329,423	A	7/1994	Scholz
5,475,317	A	12/1995	Smith
5,477,160	A	12/1995	Love
5,483,741	A	1/1996	Akram et al.

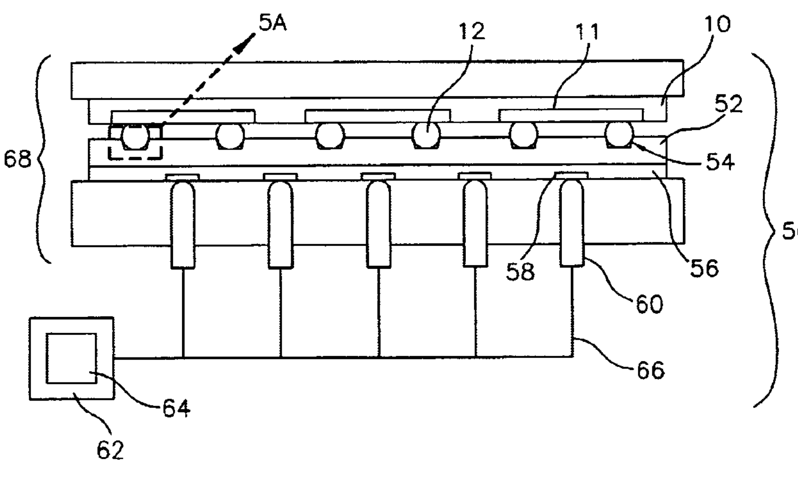
(List continued on next page.)

Primary Examiner—Kamand Cuneo
Assistant Examiner—Jimmy Nguyen
(74) *Attorney, Agent, or Firm*—Stephen A. Gratton

(57) **ABSTRACT**

A system for testing semiconductor components contained on a substrate, such as a wafer, a panel, a leadframe or a module, includes an interconnect configured to electrically engage all of the components on the substrate at the same time. The interconnect includes a switching network configured to selectively apply test signals to selected components, to electrically isolate defective components and to transmit test signals from selected groups of components. The system also includes a test apparatus, such as a wafer prober or a carrier for handling the substrate. A method for testing includes the steps of providing the interconnect having the switching network, and controlling test signals to the components using the switching network to perform various test procedures, such as functionality tests, parametric tests and burn-in tests.

55 Claims, 8 Drawing Sheets



U.S. PATENT DOCUMENTS

5,491,427 A		2/1996	Ueno et al.	
5,500,605 A		3/1996	Chang	
5,592,736 A		1/1997	Akram et al.	
5,625,298 A		4/1997	Hirano et al.	
5,686,317 A		11/1997	Akram et al.	
5,736,850 A		4/1998	Legal	
5,789,271 A		8/1998	Akram	
5,834,945 A		11/1998	Akram et al.	
5,869,974 A		2/1999	Akram et al.	
5,915,977 A		6/1999	Hembree et al.	
5,918,107 A		6/1999	Fogal et al.	
5,962,921 A		10/1999	Farnworth et al.	
6,016,060 A		1/2000	Akram et al.	
6,040,702 A		3/2000	Hembree et al.	
6,060,891 A		5/2000	Hembree et al.	
6,064,216 A		5/2000	Farnworth et al.	
6,072,321 A		6/2000	Akram et al.	
6,078,186 A		6/2000	Hembree et al.	
6,091,252 A		7/2000	Akram et al.	
6,107,109 A		8/2000	Akram et al.	
6,114,240 A		9/2000	Akram et al.	
6,127,736 A		10/2000	Akram	
6,181,144 B1		1/2001	Hembree et al.	
6,188,232 B1		2/2001	Akram et al.	
6,204,678 B1		3/2001	Akram et al.	
6,208,157 B1		3/2001	Akram et al.	
6,218,848 B1		4/2001	Hembree et al.	
6,229,324 B1		5/2001	Akram et al.	
6,232,243 B1		5/2001	Farnworth et al.	
6,239,590 B1		5/2001	Krivy et al.	
6,242,935 B1		6/2001	Akram	
6,246,245 B1		6/2001	Akram et al.	
6,246,250 B1	*	6/2001	Doherty et al.	324/765
6,261,854 B1		7/2001	Akram et al.	
6,275,052 B1		8/2001	Hembree et al.	
6,281,044 B1		8/2001	VanNortwick	
6,285,203 B1		9/2001	Akram et al.	
6,294,837 B1		9/2001	Akram et al.	
6,300,786 B1		10/2001	Doherty et al.	
6,337,577 B1	*	1/2002	Doherty et al.	324/765
6,366,112 B1		4/2002	Doherty et al.	
6,433,574 B1	*	8/2002	Doherty et al.	324/765
6,466,047 B1	*	10/2002	Doherty et al.	324/765

* cited by examiner

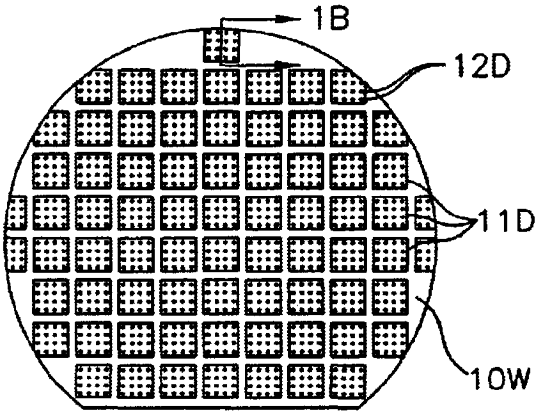


FIGURE 1A
(PRIOR ART)

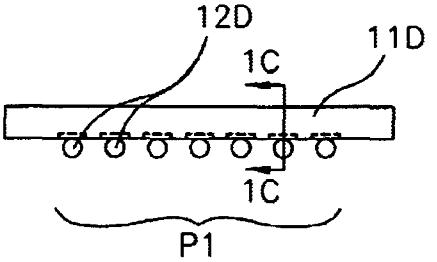


FIGURE 1B
(PRIOR ART)

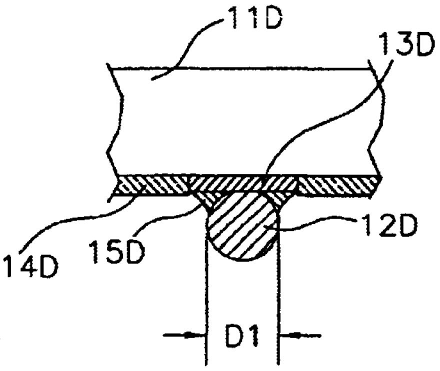


FIGURE 1C
(PRIOR ART)

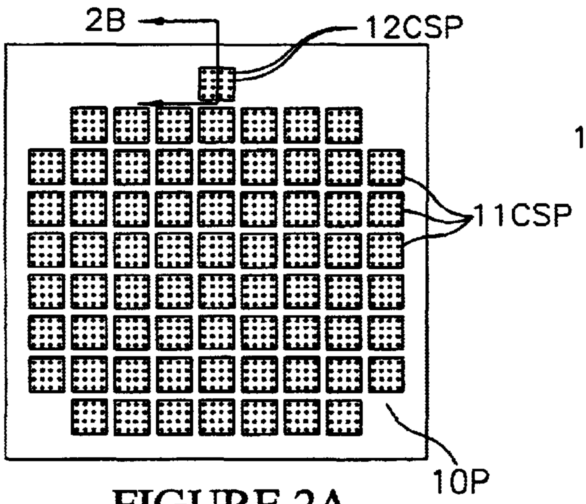


FIGURE 2A
(PRIOR ART)

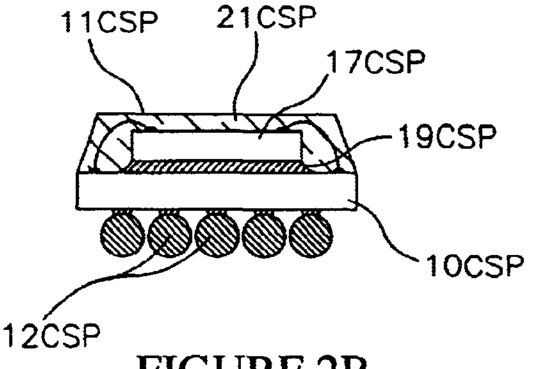


FIGURE 2B
(PRIOR ART)

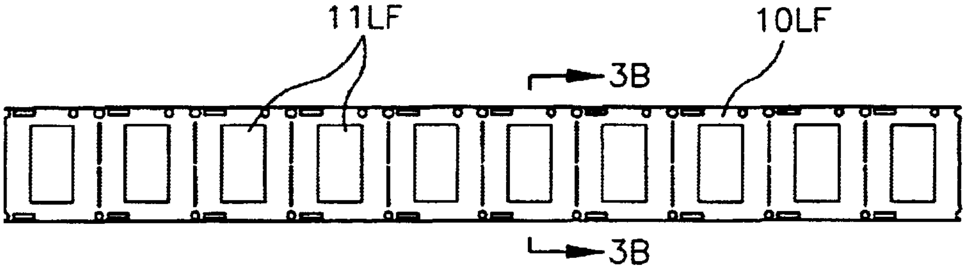


FIGURE 3A
(PRIOR ART)

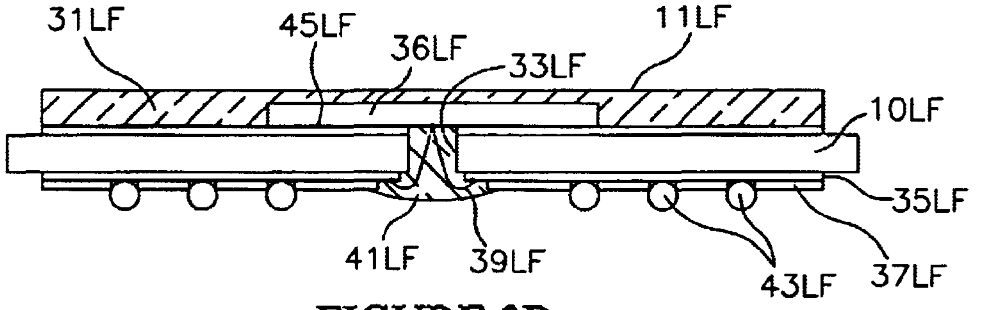


FIGURE 3B
(PRIOR ART)

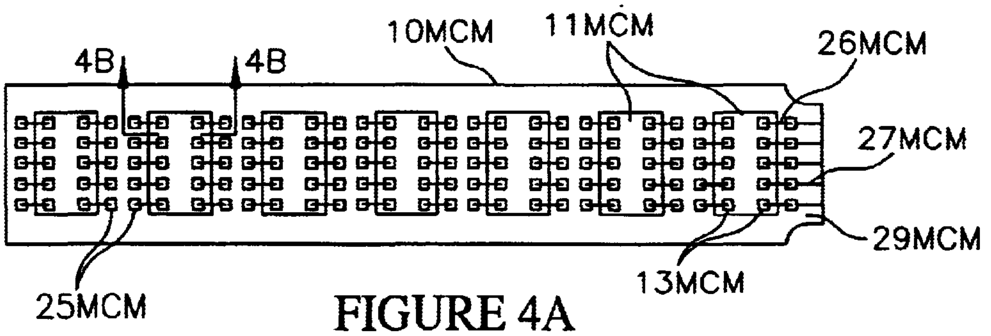


FIGURE 4A
(PRIOR ART)

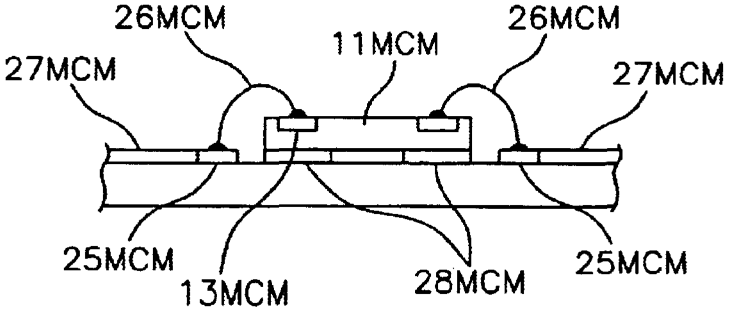


FIGURE 4B
(PRIOR ART)

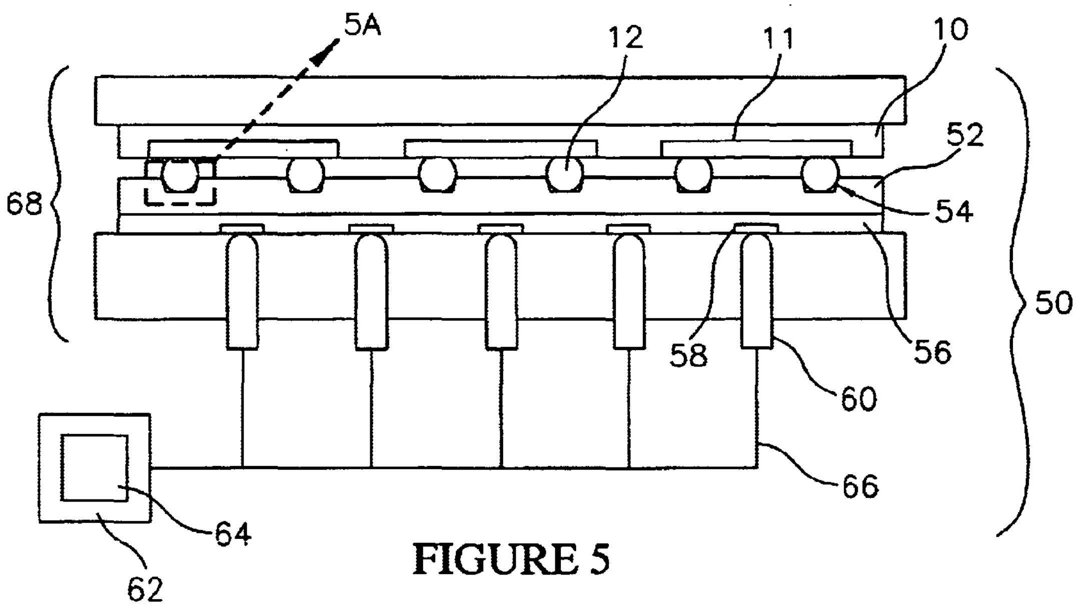


FIGURE 5

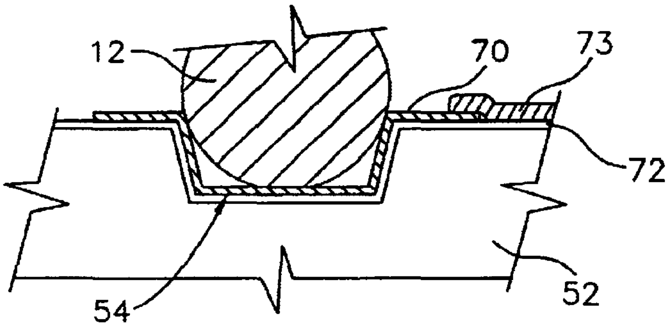


FIGURE 5A

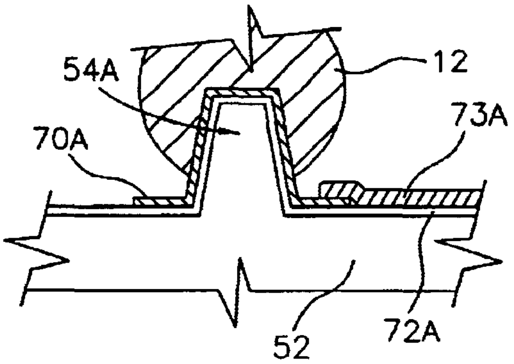


FIGURE 5B

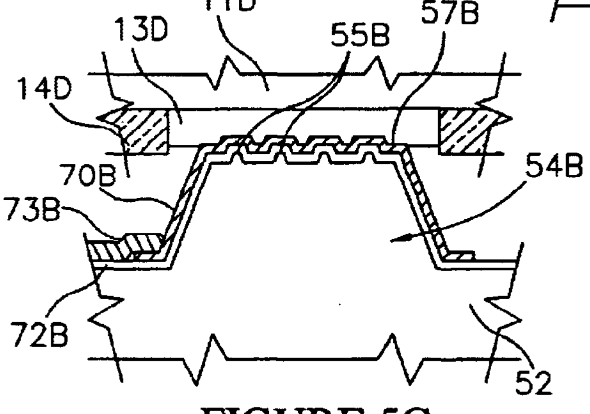
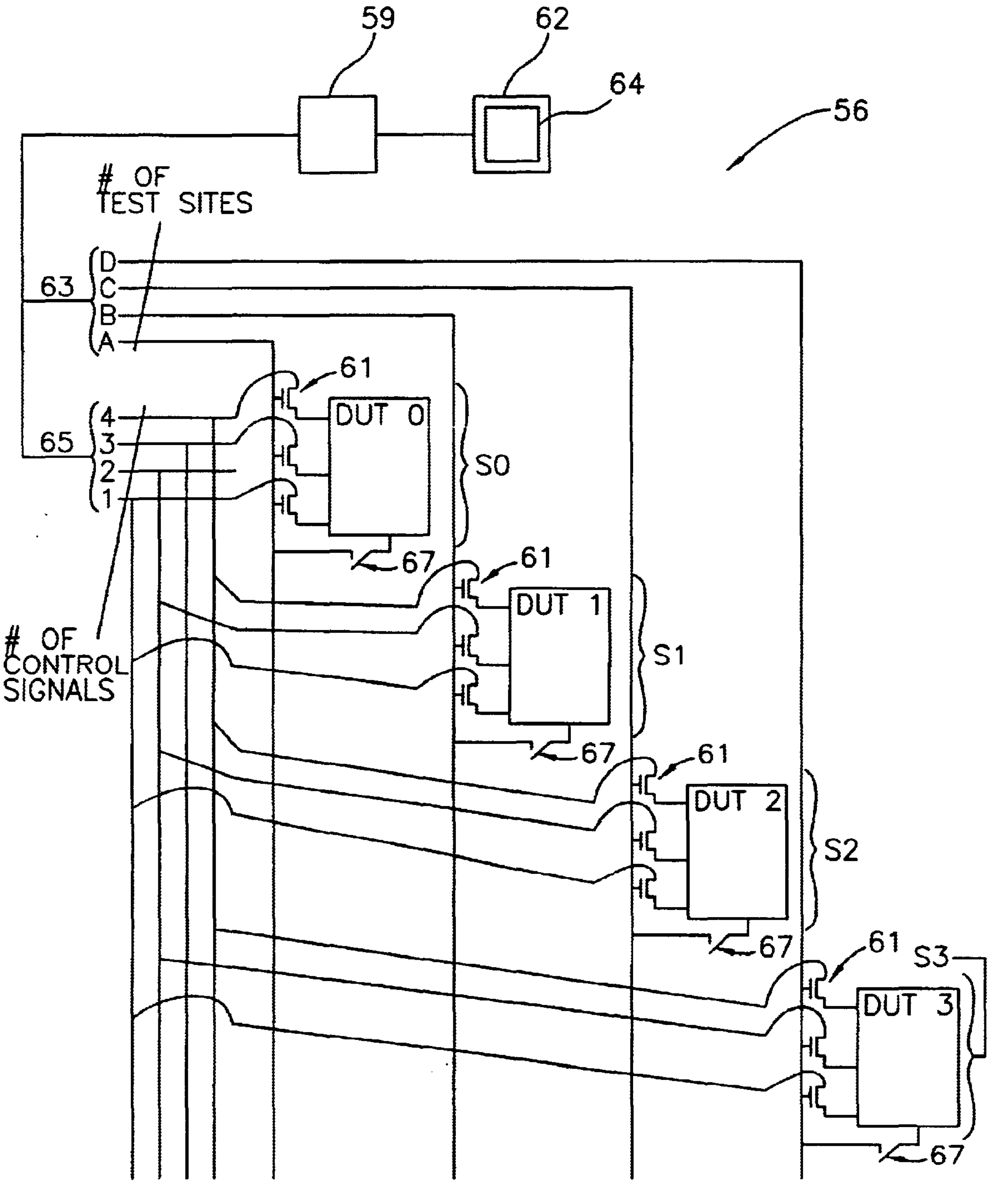


FIGURE 5C



59
62
64
56
OF TEST SITES
63
D
C
B
A
61
DUT 0
S0
65
4
3
2
1
67
61
DUT 1
OF CONTROL SIGNALS
S1
67
61
DUT 2
S2
67
61
S3
DUT 3
67

FIGURE 6

ALIGN THE COMPONENT CONTACTS 12 TO THE INTERCONNECT CONTACTS 54.

PLACE THE COMPONENT CONTACTS 12 AND THE INTERCONNECT CONTACTS 54 IN PHYSICAL AND ELECTRICAL CONTACT.

TRANSMIT TEST SIGNALS FOR PERFORMING FUNCTIONALITY TESTS (e.g., OPENS AND SHORTS) THROUGH THE INTERCONNECT CONTACTS 54 TO SELECTED COMPONENTS 11 USING THE SWITCHING NETWORK 56 TO MULTIPLY AND SELECTIVELY TRANSMIT THE TEST SIGNALS.

ELECTRICALLY ISOLATE ANY DEFECTIVE OR NONFUNCTIONAL COMPONENTS 11 USING THE SWITCHING NETWORK 56.

TRANSMIT "WRITE" TEST SIGNALS FOR PERFORMING PARAMETRIC TESTING (e.g., SPEED GRADING) THROUGH THE INTERCONNECT CONTACTS 54 TO SELECTED COMPONENTS 11 USING THE SWITCHING NETWORK 56 TO MULTIPLY AND SELECTIVELY TRANSMIT THE WRITE TEST SIGNALS.

TRANSMIT "READ" TEST SIGNALS FROM SELECTED GROUPS OF COMPONENTS 11 UP TO THE LIMIT OF TESTER RESOURCES USING THE SWITCHING NETWORK 56 TO GROUP THE COMPONENTS 11 AS REQUIRED.

OPTIONALLY, TRANSMIT BURN-IN TEST SIGNALS TO THE COMPONENTS 11 USING THE SWITCHING NETWORK 56 TO ELECTRICALLY ISOLATE DEFECTIVE COMPONENTS 11.

FIGURE 7

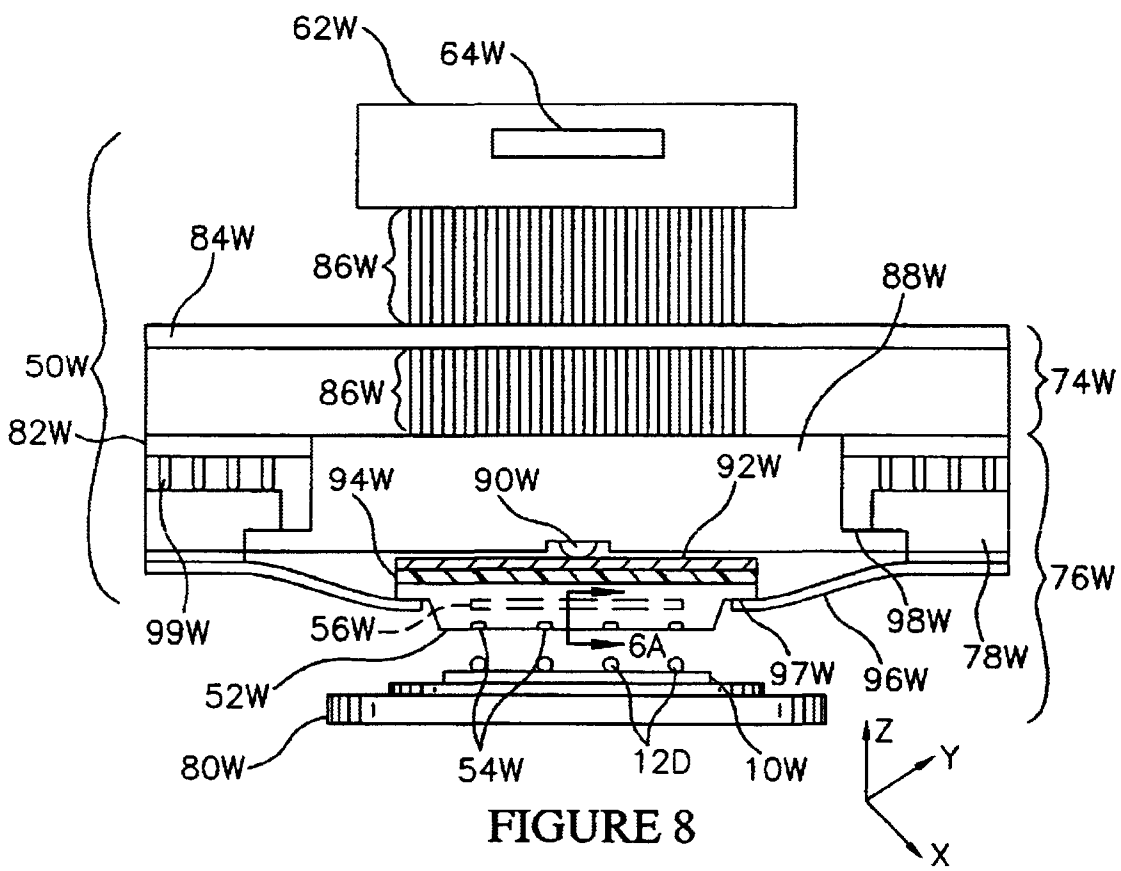


FIGURE 8

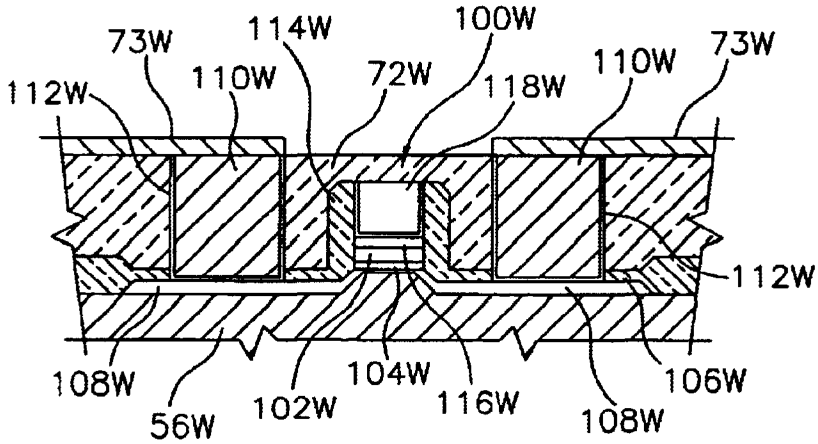


FIGURE 8A

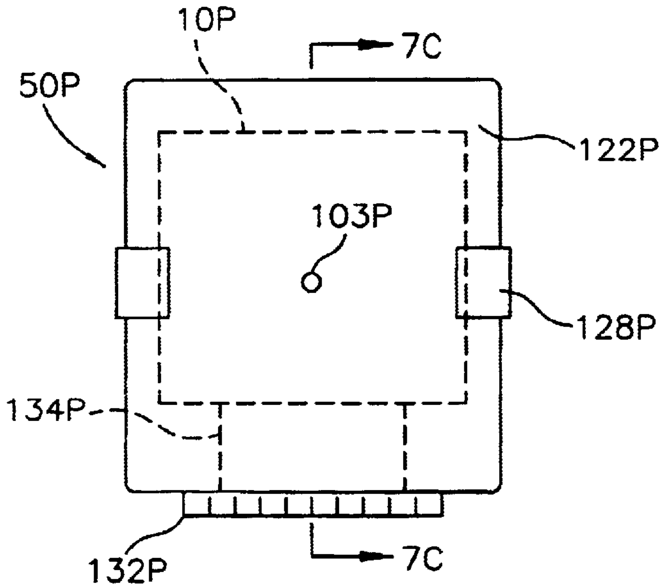


FIGURE 9A

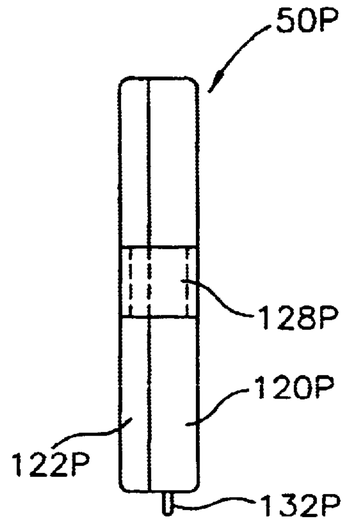


FIGURE 9B

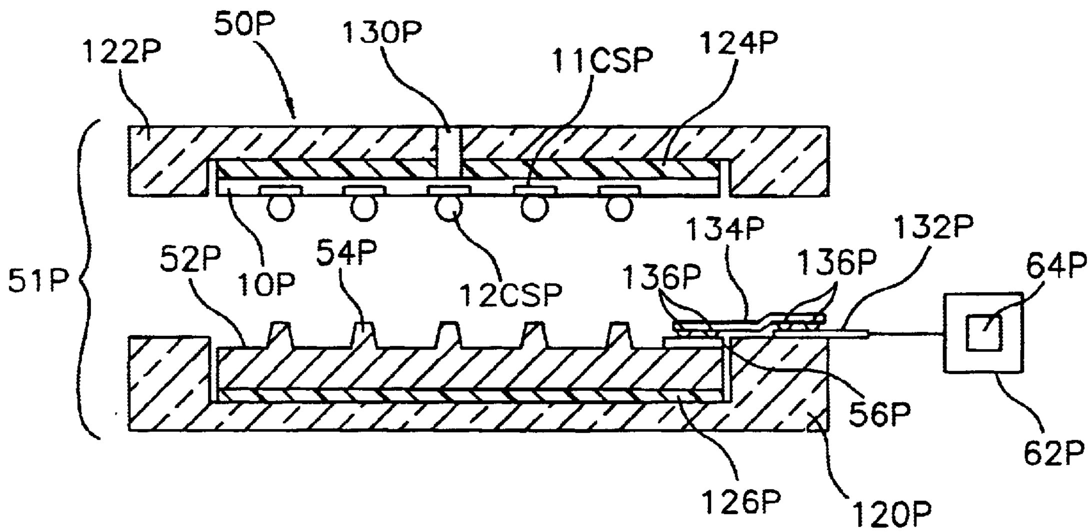


FIGURE 9C

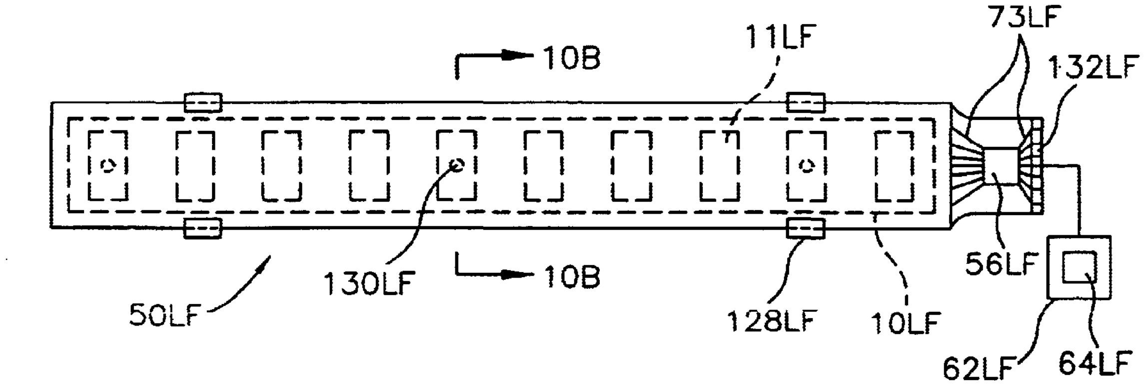


FIGURE 10A

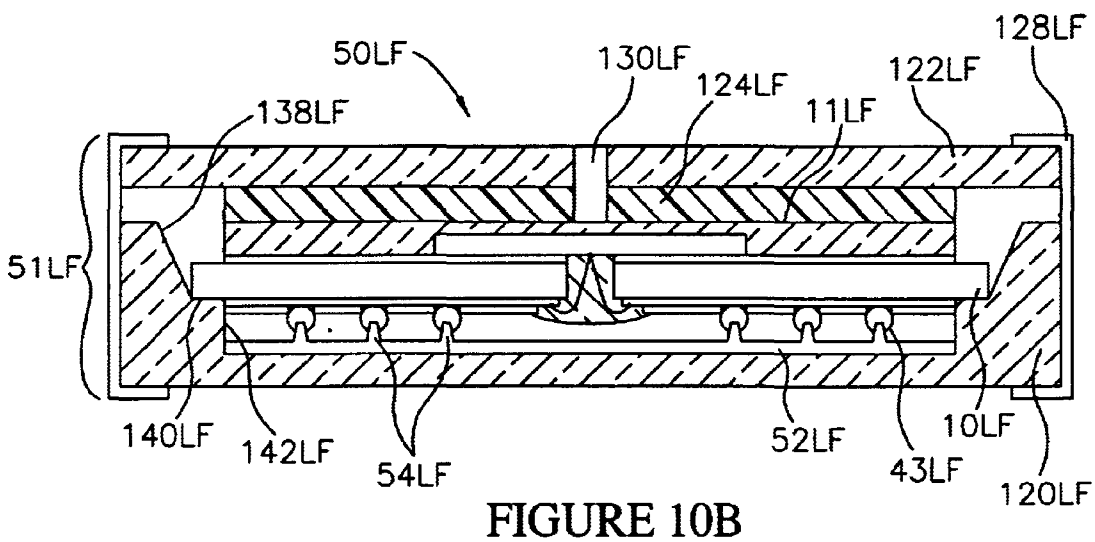


FIGURE 10B

METHOD AND SYSTEM HAVING SWITCHING NETWORK FOR TESTING SEMICONDUCTOR COMPONENTS ON A SUBSTRATE

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation-in-part of Ser. No. 09/999,502, filed Dec. 4, 2001, U.S. Pat. No. 6,466,047 B1, which is a division of Ser. No. 09/675,072, filed Sep. 28, 2000, U.S. Pat. No. 6,433,574 B1, which is a division of Ser. No. 09/244,373, filed Feb. 4, 1999, U.S. Pat. No. 6,337,577, which is a continuation-in-part of Ser. No. 09/075,691, filed May 11, 1998, U.S. Pat. No. 6,246,250.

FIELD OF THE INVENTION

This invention relates generally to semiconductor manufacture, and specifically to a method and system for testing semiconductor components.

BACKGROUND OF THE INVENTION

Semiconductor components are typically fabricated on a common substrate which is then singulated into individual components. Semiconductor dice, for example, are fabricated on a semiconductor wafer. Semiconductor packages can be fabricated on a wafer, on a leadframe or on a panel. Some types of semiconductor components, such as multi chip modules and memory modules, also include multiple components contained on a common substrate.

Following the fabrication process, the components are tested. For testing the components, temporary electrical connections are made with terminal contacts on the components, and test signals are transmitted to the integrated circuits on the components. The testing procedures can be performed using a test system in which an interconnect of the system, such as a probe card, makes the temporary electrical connections with the terminal contacts on the components. A typical test system for semiconductor wafers includes a wafer prober for handling and positioning the wafers, a tester for generating and analyzing test signals, a probe card for making temporary electrical connections with the wafer, and a prober interface board for routing test signals from the tester pin electronics to the probe card.

With prior art testing processes, the components are typically tested one component at a time. With wafer testing for example, either the wafer or the probe card is stepped, such that only one die at a time is electrically engaged and tested. The stepping process takes additional time and introduces an additional variable in making the temporary electrical connections with the dice. Other prior art testing processes test the components after singulation from the substrate. Semiconductor packages and BGA devices, for example, are typically tested in singulated form.

The present invention is directed to a method and system for testing multiple components contained on a common substrate at the same time. The method and system can be used for testing components contained on a variety of substrates including wafers, panels, leadframes and modules.

SUMMARY OF THE INVENTION

In accordance with the present invention, a method and a system for testing semiconductor components contained on a substrate are provided. The method uses a switching network for multiplying and controlling the transmission of

test signals from a tester to the components on the substrate. The switching network also electrically isolates defective components, and allows selective transmission of read test signals from selected components or groups of components on the substrate for expanding tester resources. The switching network can be used to control test signals for performing functionality tests, parametric tests and burn-in tests on the components.

The system includes the substrate containing the components, a test apparatus for handling the substrate, and the tester for applying the test signals to the components. The test apparatus includes the interconnect which includes interconnect contacts for making temporary electrical connections with the component contacts, and the switching network for controlling test signals to and from the interconnect contacts during testing of the components.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1**A is a schematic plan view of a prior art wafer substrate containing semiconductor components in the form of dice;

FIG. **1**B is an enlarged cross sectional view taken along section line **1**B—**1**B of FIG. **1**A illustrating a component on the wafer substrate;

FIG. **1**C is an enlarged cross sectional view taken along section line **1**C—**1**C of FIG. **1**B illustrating a bumped contact;

FIG. **2**A is a schematic plan view of a prior art panel substrate containing semiconductor components in the form of chip scale packages;

FIG. **2**B is an enlarged cross sectional view taken along section line **2**B—**2**B of FIG. **2**A illustrating a component on the panel substrate;

FIG. **3**A is a schematic plan view of a prior art leadframe substrate containing semiconductor components in the form of packages;

FIG. **3**B is an enlarged cross sectional view taken along section line **3**B—**3**B of FIG. **3**A illustrating a component on the leadframe substrate;

FIG. **4**A is a schematic plan view of a prior art module substrate containing semiconductor components in the form of dice or packages;

FIG. **4**B is an enlarged cross sectional view taken along section line **4**B—**4**B of FIG. **4**A illustrating a component on the module substrate;

FIG. **5** is a schematic diagram of a generic test system constructed in accordance with the invention;

FIG. **5**A is an enlarged cross sectional view taken along line **5**A of FIG. **5** illustrating an interconnect contact;

FIG. **5**B is an enlarged cross sectional view equivalent to FIG. **5**A of an alternate embodiment interconnect contact;

FIG. **5**C is an enlarged cross sectional view equivalent to FIG. **5**A of an alternate embodiment interconnect contact;

FIG. **6** is an electrical schematic diagram illustrating a switching network of the test system;

FIG. **7** is a block diagram illustrating steps in the method of the invention;

FIG. **8** is a schematic diagram of a wafer test system constructed in accordance with the invention;

FIG. **8**A is an enlarged cross sectional view taken along line **8**A of FIG. **8** illustrating an FET transistor of the switching network on an interconnect of the wafer test system;

FIG. **9**A is a schematic plan view of a panel test system constructed in accordance with the invention;

FIG. **9**B is a side elevation view of FIG. **9**A;

FIG. **9**C is an enlarged schematic cross sectional view taken along section line **9**C of FIG. **9**A;

FIG. **10**A is a schematic plan view of a leadframe test system constructed in accordance with the invention; and

FIG. **10**B is an enlarged schematic cross sectional view taken along section line **10**B of FIG. **10**A.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

As used herein, the term "semiconductor component" means an electronic element that includes a semiconductor die. Exemplary semiconductor components include semiconductor dice, semiconductor packages, semiconductor wafers, BGA devices, multi chip modules and circuit boards.

The term "substrate" means a base element on which multiple components are mounted or contained. Exemplary substrates include wafers or portions thereof, leadframes, panels, module substrates and boards.

The term "write test signal" means an electronic signal transmitted from a tester to a device under test.

The term "read test signal" means an electronic signal transmitted from a device under test to a tester.

Referring to FIGS. **1**A–**1**C, **2**A–**2**B, **3**, **4**A and **4**B, various prior art substrates containing semiconductor components are illustrated. As will be further explained, the method and system of the invention can be used to test each of the substrates and the components thereon, as well as other types of substrates, which contain semiconductor components.

In FIG. **1**A, a wafer substrate **10**W, such as a semiconductor wafer, includes a plurality of components **11**D such as semiconductor dice. The wafer substrate **10**W comprises a semiconducting material such as silicon or gallium arsenide. FIG. **1**B illustrates a component **11**D that has been separated from the wafer substrate **10**W. The component **11**D includes an array of component contacts **12**D, such as metal balls or bumps, formed on a face thereof. The component contacts **12**D are formed in a selected pattern **P1**, such as a dense ball grid array (BGA).

As shown in FIG. **1**C, the component contacts **12**D are bonded to bond pads **13**D on the component **11**D. The bond pads **13**D are in electrical communication with the integrated circuits contained on the component **11**D. In addition, the bond pads **13**D are surrounded by a passivation layer **14**D formed on the face of the component **11**D. As also shown in FIG. **1**C, fillets **15**D attach the component contacts **12**D to the bond pads **13**D.

Referring to FIG. **2**A, a panel substrate **10**P includes a plurality of semiconductor components **11**CSP, such as chip scale packages. The panel substrate **10**P comprises an electrically insulating material such as ceramic, a reinforced polymer laminate, such as bismaleimide triazine (BT), or an epoxy resin (e.g., FR-4).

As shown in FIG. **2**B, each component **11**CSP includes a component substrate **10**CSP. The component substrate **10**CSP comprises a segment of the panel substrate **10**P which has been cut, sheared, punched or otherwise separated from a remainder of the panel substrate **10**P. In addition, each component **11**CSP includes a semiconductor die **17**CSP wire bonded to the component substrate **10**CSP, an adhesive layer **19**CSP which attaches the die **17**CSP to the component substrate **10**CSP, and an encapsulating resin **21**CSP encapsulating the die **17**CSP. Each component **11**CSP also includes an array of component contacts **12**CSP in electrical communication with the integrated circuits contained on the die **17**CSP.

The component contacts **12**CSP are formed on the component substrate **10**CSP in a dense grid array, such as a ball grid array (BGA), or a fine ball grid array (FBGA). By way of example, a representative diameter **D1** for the component contacts **12**CSP can be about 0.005-in (0.127 mm) to 0.050-in (1.270 mm) or greater. A representative pitch P (center to center spacing) of the component contacts **12**CSP can be from about 0.008-in (0.228 mm) to about 0.060-in (1.524 mm) or greater.

Referring to FIGS. **3**A and **3**B, a leadframe substrate **10**LF such as a leadframe, includes a plurality of semiconductor components **11**LF, such as BGA devices. In the illustrative embodiment, the leadframe substrate **10**LF comprises a polymer material, such as a reinforced polymer laminate (e.g., bismaleimide triazine (BT) polyimide). Alternately, a leadframe substrate can comprise a metal, such as a nickel-iron alloy, a copper alloy, or a clad stainless steel.

As shown in FIG. **3**B, each component **11**LF includes a portion of the leadframe substrate **10**LF. In addition, each component **11**LF includes a semiconductor die **36**LF, and an encapsulating resin **31**LF which encapsulates the die **36**LF. An adhesive layer **45**LF bonds the die **36**LF to the leadframe substrate **10**LF in a board-on-chip configuration. In addition, wires **39**LF are wire bonded through an opening **33**LF in the leadframe substrate **10**LF, to the die **36**LF and to conductors **35**LF on the leadframe substrate **10**LF. Further, a glob top encapsulant **41**LF encapsulates the wires **39**LF and associated wire bonds. The components **11**LF also include solder masks **37**LF on the conductors **35**LF, and solder balls **43**LF in electrical communication with the conductors **35**LF. The solder balls **43**LF are arranged in a dense grid array, such as a ball grid array or fine ball grid array.

Referring to FIGS. **4**A and **4**B, a module substrate **10**MCM, such as a multi chip module, includes a plurality of semiconductor components **11**MCM in the form of semiconductor dice, or alternately semiconductor packages. The module substrate **10**MCM comprises an electrically insulating material, such as ceramic, or plastic. Adhesive members **28**MCM attach the components **11**MCM to the module substrate **10**MCM. In addition, the module substrate **10**MCM includes electrodes **25**MCM which are electrically connected to bond pads **13**MCM on the components **11**MCM. Wires **26**MCM are wire bonded to the electrodes **25**MCM and to the bond pads **13**MCM to form separate electrical paths therebetween. The module substrate **10**MCM also includes conductive traces **27**MCM, and an edge connector **29**MCM in electrical communication with the electrodes **25**MCM. The module substrate **10**MCM, components **11**MCM and conductive traces **27**MCM can be configured as a memory module or other electronic element having a desired configuration.

Test System

Referring to FIG. **5**, a generic test system **50** constructed in accordance with the invention is illustrated. The test system **50** is adapted to test semiconductor components **11** contained on a substrate **10** and having component contacts **12**. The substrate **10** and the components **11** can be in any one of the previously described configurations, such as the wafer substrate **10**W and the components **11**D of FIGS. **1**A–**1**C, the panel substrate **10**P and the components **11**CSP of FIGS. **2**A–**2**B, the leadframe substrate **10**LF and the components **11**LF of FIGS. **3**A–**3**B, or the module substrate **10**MCM and the components **11**MCM of FIGS. **4**A–**4**B.

The test system **50** includes an interconnect **52** which comprises a plurality of interconnect contacts **54**. The interconnect contacts **54** are configured to make temporary

electrical connections with all of the component contacts **12** on all of the components **11** contained on the substrate **10** at the same time. These temporary electrical connections can be used to apply test signals to the integrated circuits contained on the semiconductor components **11**.

The test system **50** also includes a switching network **56** on the interconnect **52** in electrical communication with the interconnect contacts **54**. The switching network **56** is configured to multiply (i.e., fan out), and to selectively transmit, "write" test signals to selected components **11**, or to selected groups of components **11**, on the substrate **10** in response to control signals. The switching network **56** is also configured to selectively transmit "read" test signals from selected groups of components **11** for expanding tester resources. In addition, the switching network **56** is configured to electrically isolate or disconnect defective components **11**. As will be further explained, the switching network **56** includes integrated circuitry and active electrical switching devices, such as FETs, operable by control signals generated by a controller.

The test system **50** also includes a tester **62** and electrical connectors **60** in electrical communication with the tester **62**. The tester **62** includes test circuitry **64** configured to generate and transmit "write" test signals through the switching network **56** to the components **11**. In addition, the tester **62** is configured to analyze "read" test signals transmitted from the components **11** and through the switching network **56**. The electrical characteristics of the test signals, and the configuration of the tester **62** will depend on the test procedures being performed. Exemplary test procedures include functionality tests, such as tests for opens and shorts, parametric tests such as speed grading, and burn-in tests wherein the components **11** are heated and test signals are applied. Depending on the components **11**, suitable testers **62** are commercially available from Teradyne of Boston, Mass., as well as other manufacturers.

The tester **62** also includes a plurality of separate electrical paths **66** to the electrical connectors **60**. The signal generating and analyzing capability of the tester **62**, and the number of separate electrical paths **66** provided by the tester **62**, are termed herein as "tester resources". In general, the configurations of the test circuitry **64**, and of the electrical paths **66**, are fixed for a particular tester **62** by the manufacturer. For example, the test circuitry **64** can be configured to route drive only signals through some of the electrical paths **66**, and input/output channels through other of the electrical paths **66**, as required for testing a particular type of component **11**.

The test system **50** also includes a testing apparatus **68** configured to retain and align the substrate **10** with the interconnect **52**. The testing apparatus **68** also functions to bias the substrate **10** and the interconnect **52** together with a force sufficient to establish the temporary electrical connections between the interconnect contacts **54** and the component contacts **12**. The configuration of the testing apparatus **50** is dependent on the substrate **10**, the components **11** being tested, and the test procedures being performed. For example, for testing the wafer substrate **10**W (FIG. **1**A) the testing apparatus **50** can comprise a wafer prober. For testing the panel substrate **10**P (FIG. **2**A) or the leadframe substrate **10**LF, the testing apparatus can comprise a test carrier.

Referring to FIG. **5**A, a single interconnect contact **54** is illustrated. In the illustrative embodiment, the interconnect **52** comprises silicon and the interconnect contacts **54** comprise conductive pockets configured to retain and electrically engage the component contacts **12**. In addition, the interconnect contacts **54** include conductive layers **70** on the pockets, and the interconnect **52** includes patterns of conductors **73** in electrical communication with the conductive layer **70**. The conductors **73** establish electrical communication between the interconnect contacts **54** and the multiplex contacts **58**, and with other electrical elements on the interconnect **52** as required. The conductive layers **70** and the conductors **73** can comprise a metal such as aluminum, titanium, nickel, iridium, copper, gold, tungsten, silver, platinum, palladium, tantalum, molybdenum or alloys of these metal. The interconnect **52** also includes an insulating layer **72** for electrically insulating the interconnect contacts **54**, the conductive layers **70** and the conductors **73** from the bulk of the interconnect **52**. The interconnect contacts **54** and conductors **73** can be fabricated as described in U.S. Pat. No. 6,107,109 to Akram et al., which is incorporated herein by reference.

Referring to FIG. **5**B, alternate embodiment interconnect contacts **54**A are configured to penetrate the component contacts **12** to form the temporary electrical connections. In this embodiment the interconnect comprises silicon, and the interconnect contacts **54**A comprise projections covered with conductive layers **70**A in electrical communication with conductors **73**A, and electrically insulated by an insulating layer **72**A. The interconnect contacts **54**A and the conductors **73**A can be fabricated as described in U.S. Pat. No. 5,686,317 to Akram et al., and in U.S. Pat. No. 5,686,317 to Akram et al., both of which are incorporated herein by reference.

Referring to FIG. **5**C, alternate embodiment interconnect contacts **54**B are configured to electrically engage planar component contacts, such as bond pads **13**D on the component **11**D. In this embodiment, the interconnect **52** comprises silicon, and the interconnect contacts **54**B comprise raised members that project from a surface of the interconnect **52**. In addition, the interconnect contacts **54**B include penetrating projections **55**B adapted to penetrate the bond pads **13**D to a limited penetration depth. To limit the penetration depth, the penetrating projections **55**B have a height that is less than a thickness of the bond pads **13**D. In addition, surfaces **57**B at the tips of the interconnect contacts **54**B provide stop planes for limiting penetration into the bond pads **13**D. In addition, each interconnect contact **54**B is covered with a conductive layer **70**B in electrical communication with a conductor **73**B. Further, an insulating layer **72**B electrically insulates the conductive layers **70**B and the conductors **73**B. A process for fabricating the interconnect contacts **54**B on a silicon substrate, substantially as shown in FIG. **5**C is described in previously cited U.S. Pat. No. 5,483,741, to Akram et al., and U.S. Pat. No. 5,686,317 to Akram et al.

Switching Network

Referring to FIG. **6**, the switching network **56** of the test system **50** is illustrated. The switching network **56**, simply stated, comprises a grid of active electrical switching devices **61**, such as field effect transistors (FETs) configured to control the transmission of signals from the tester **62** (FIG. **5**) to the components **11**. The components **11** being tested are termed herein as devices under test (DUTs).

The switching network **56** includes a plurality of test sites **S0**, **S1**, **S2**, **S3** etc., each of which is configured to test a DUT (e.g., DUT **0**, DUT **1**, DUT **3**, DUT **4** etc). Each test site **S0**, **S1**, **S2**, **S3** etc., includes a plurality of active electrical switching devices **61** in electrical communication with the interconnect contacts **54** (FIG. **5**). For simplicity each test site **S0**, **S1**, **S2**, **S3** etc. is illustrated with only three active electrical switching devices **61**. Each test site **S0**, **S1**, **S2**, **S3** etc., also includes at least one on-off switch **67**.

The switching network **56** includes a master site control **63** in electrical communication with a controller **59**. The

master site control **63** includes a plurality of separate control lines A, B, C, D etc. Each test site S**0**, S**1**, S**2**, S**3** etc. has an associated control line A, B, C, D etc. in electrical communication with the gate elements of the active electrical switching devices **61** for the test site. The master site control **63** is operable by the controller **59** to electrically connect or isolate the test sites S**0**, S**1**, S**2**, S**3** etc. by selective operation of the gate elements of the active electrical switching devices **61**. In particular, the master site control **63** is operable by the controller **59** to place the active electrical switching devices **61** in either an "on" condition or an "off" condition.

The switching network **56** also includes a signal control **65** having control lines 1, 2, 3, 4 etc. in electrical communication with the sources or drains of the active electrical switching devices **61**. The signal control **65** can be used to write all of the DUTs at the same time, and to place all of the DUTs in a selected mode at the same time. For example, if the DUTs comprise DRAMs the signal control **65** can be used to place all of the DUTs in a refresh mode. The signal control **65** can also be used to selectively read signals from the DUTs individually, or in groups. The signal control **65** can also be used to selectively transmit "write" test signals from the tester **62** to selected DUTS, or groups of DUTs, and to selectively transmit "read" test signals from selected DUTs or groups of DUTs.

Test Method

Referring to FIG. **7**, steps in a method for testing the components **11** on the substrate **10** using the test system **50** of FIG. **5** are illustrated.

1. Align the component contacts **12** to the interconnect contacts **54**.
2. Place the component contacts **12** and the interconnect contacts **54** in physical and electrical contact.
3. Transmit test signals for performing functionality tests (e.g., opens and shorts) through the interconnect contacts **54** to selected components **11** using the switching network **56** to multiply and selectively transmit the test signals.
4. Electrically isolate any defective or non-functional components **11** using the switching network **56**.
5. Transmit "write" test signals for performing parametic testing (e.g., speed grading) through the interconnect contacts **54** to selected components **11** using the switching network **56** to multiply and selectively transmit the write test signals.
6. Transmit "read" test signals from selected groups of components **11** up to the limit of tester resources using the switching network **56** to group the components **11** as required.
7. Optionally, transmit burn-in test signals to the components **11** using the switching network **56** to electrically isolate defective components **11**.

Wafer Test System

Referring to FIG. **8**, a wafer test system **50**W constructed in accordance with the invention, and configured to test components **11**D (FIG. **1**A) contained on the wafer substrate **10**W is illustrated. The wafer test system **50**W includes a test head **74**W and an interconnect **52**W. The interconnect **52**W includes patterns of interconnect contacts **54**W configured to make temporary electrical connections with the component contacts **12**D. The interconnect **52**W also includes a switching network **56**W in electrical communication with the interconnect contacts **54**W.

The wafer test system **50**W also includes a wafer prober **76**W wherein the interconnect **52**W is mounted, and a tester **62**W having test circuitry **64**W configured to apply test signals through the interconnect **52**W, to the components **11**D contained on the wafer substrate **10**W, and to analyze the resultant signals. The wafer prober **76**W includes an interconnect holder **78**W for mounting and electrically interfacing with the interconnect **52**W.

The wafer prober **76**W also includes a wafer chuck **80**W configured to move in X and Y directions to align the wafer substrate **10**W with the interconnect **52**W, and in the Z direction to move the wafer substrate **10**W into contact with the interconnect **52**W. One suitable wafer prober **76**W is manufactured by Electroglass and is designated a Model 4080.

The test system **50**W also includes a prober interface board **82**W for routing test signals from the test head **74**W to the interconnect **52**W. In addition, the prober interface board **82**W can be in electrical communication with tester pin electronics **84**W in the test head **74**W. The tester pin electronics **84**W provide separate electrical paths **86**W from the test circuitry **64**W contained in the tester **62**W, to the test head **74**W and to the prober interface board **82**W.

Still referring to FIG. **8**, the wafer prober **76**W also includes a force applying fixture **88**W and a force applying mechanism **90**W. These items can be components of a conventional wafer prober as previously described. The force applying mechanism **90**W presses against a pressure plate **92**W and a compressible member **94**W to bias the interconnect **52**W against the wafer substrate **10**W. By way of example, the compressible member **94**W can be formed of an elastomeric material such as silicone, butyl rubber, or fluorosilicone; in foam, gel, solid or molded configurations.

In addition, a flexible membrane **96**W is bonded to the interconnect **52**W and to the interconnect holder **78**W In general, the flexible membrane **96**W functions to physically attach the interconnect **52**W to the interconnect holder **78**W. In addition, the flexible membrane **96**W functions to provide electrical paths between the switching network **56**W, the interconnect contacts **54**W and the test circuitry **64**W of the tester **62**W. The flexible membrane **96**W can be formed of thin flexible materials to allow movement of the interconnect **52**W in Z-directions. For example, the flexible membrane **96**W can be formed of a flexible multi layered material similar to TAB tape.

In the illustrative embodiment, the flexible membrane **96**W comprises a layer of polymer tape having metal conductors thereon. Bonded connections are formed between the conductors on the membrane **96**W and corresponding conductors **98**W on the interconnect holder **78**W. In addition, bonded connections are formed between the conductors on the membrane **96**W and bonding pads **97**W on the interconnect **52**W.

Still referring to FIG. **8**, the wafer prober **76**W includes spring loaded electrical connectors **99**W which are in electrical communication with the prober interface board **82**W. One type of spring loaded electrical connector **99**W is manufactured by Pogo Industries of Kansas City, Mo. under the trademark "POGO PINS". The electrical connectors **99**W electrically communicate with the conductors **98**W on the interconnect holder **78**W.

The interconnect mounting arrangement shown in FIG. **8**, as well as others, are described in U.S. Pat. No. 6,060,891, to Hembree et al., which is incorporated herein by reference. However, it is to be understood that these mounting arrangements are merely exemplary, and the interconnect **52**W can be mounted in any conventional manner.

In the embodiment illustrated in FIG. **8**, the interconnect **52**W comprises a semiconductor material, such as silicon,

and the switching network **56**W is formed in the semiconductor material using semiconductor fabrication techniques. As such, the interconnect **52**W includes active electrical switching devices, such as FET transistors, formed integrally with the semiconductor material.

For example, the switching network **56**W can include FET transistor constructed substantially as shown in FIG. **8**A for transistor **100**W. However, as is apparent the FET transistor **100**W is merely one component of the switching network **56**W, and the switching network **56**W can include additional components to function in the previously described manner. Further, other active electrical switching devices, such as NPN or PNP transistors can be used in place of the FET transistor **100**W illustrated in FIG. **6**A.

The FET transistor **100**W includes a polysilicon gate **102**W, and a gate oxide **104**W. In addition, an isolation structure **106**W, such as a field oxide or an isolation trench is formed on the interconnect **56**W for electrically isolating the FET transistor **100**W from adjacent transistors. The FET transistor **100**W also includes N+active areas **108**W, which can be formed by implanting dopants into the interconnect **56**W to form the source and drain of the FET transistor **100**W. Metal filled vias **110**W with metal silicide layers **112**W, electrically connect the source and drain of the FET transistor **100**W to conductors **73**W in electrical communication with the interconnect contacts **54**W (FIG. **8**) and the bonding pads **97**W (FIG. **8**). In addition, an insulating layer **72**W electrically insulates the conductors **73**W, the interconnect contacts **54**W and the bonding pads **97**W. The FET transistor **100**W also includes spacers **114**W, TEOS layers **116**W and nitride caps **118**W.

Panel Test System

Referring to FIGS. **9**A–**9**C, a panel test system **50**P constructed in accordance with the invention is illustrated. The panel test system **50**P can be used to perform functionality, parametic and burn-in testing of the previously described components **11**CSP contained on the panel substrate **10**P. These tests can be performed sequentially or separately using the panel test system **50**P. The panel test system **50**P can also be used to test the components **11**MCM contained on the multi chip module substrate **10**MCM.

The panel test system **50**P includes a carrier **51**P for holding and applying the required test signals to the components **11**CSP. These test signals can include functionality test signals, parametric test signals and burn-in test signals. For performing burn-in testing the carrier **51**P can be placed in a burn-in oven configured to heat the components **11**CSP to a required temperature for a required time period.

The carrier **51**P includes a base **120**P; a cover **122**P; an interconnect **52**P (FIG. **9**C); and a force applying member in the form of elastomeric spring members **124**P and **126**P (FIG. **9**C). The base **120**P and the cover **122**P comprise an insulating material such as molded plastic or laminated ceramic, and are adapted for mating physical engagement. In addition, the base **120**P and the cover **122**P have a size that corresponds to the size of the panel substrate **10**P. Clip members **128**P removably secure the cover **122**P to the base **120**P with the panel substrate **10**P therein. In addition, one or more vacuum openings **130**P are formed in the cover **122**P and in the spring member **124**P, for securing the panel substrate **10**P to the cover **122**P during alignment and assembly of the panel test system **50**P.

As shown in FIG. **9**C, the base **120**P can include a cavity for mounting the interconnect **52**P and elastomeric spring member **126**P. In a similar manner, the cover **124**P can include a cavity for mounting the panel substrate **10**P and the elastomeric spring member **124**P. The elastomeric spring members **124**P, **126**P can comprise a material such as silicone, butyl rubber, or fluorosilicone.

The base **120**P also includes an electrical connector **132**P in the form of a male or female connector adapted for mating electrical engagement with a corresponding connector formed on a testing apparatus. In addition, an electrical path can be formed between the interconnect **52**P and the electrical connector **132**P by a length of TAB (tape automated bonding) tape **134**P. One type of TAB tape comprises a layer of polyimide having a desired pattern of metal conductors formed thereon. The conductors can include metal bumps **136**P formed in vias through the polyimide and arranged in a desired pattern. The metal bumps **136**P on the TAB tape **134**P can be bonded, using heat or ultrasound, to corresponding connection points on the interconnect **52**P and on the electrical connector **132**P to form an electrical connection therebetween. Alternately this electrical connection can be formed by wire bonding or mechanical electrical connectors.

As shown schematically in FIG. **9**C, the interconnect **52**P includes interconnect contacts **54**P and a switching network **56**P in electrical communication with the interconnect contacts **54**P. The interconnect contacts **54**P are constructed as previously described for interconnect contacts **54**A (FIG. **5**B) and are adapted to form temporary electrical connections with the component contacts **12**CSP on the components **11**CSP.

The panel test system **50**P also includes a tester **62**P having test circuitry **64**P. In this case, the tester **62**P can comprise a test board having a socket configured to electrically engage the electrical connector **132**P. Assembly and alignment of the panel substrate **10**P in the panel test system **50**P can be performed as described in U.S. Pat. No. 6,064, 216, to Farnworth et al., which is incorporated herein by reference.

Leadframe Test System

Referring to FIGS. **10**A–**10**B, a leadframe test system **50**LF constructed in accordance with the invention is illustrated. The leadframe test system **50**LF can be used to perform functionality, parametic and burn-in testing of the previously described components **11**LF contained on the leadframe substrate **10**LF. These tests can be performed sequentially or separately.

The leadframe test system **50**LF includes a carrier **51**LF configured to hold the leadframe substrate **10**LF for testing and to apply the required test signals to the components **11**LF. These test signals can include functionality test signals, parametric test signals and burn-in test signals. For performing burn-in testing the carrier **51**LF can be placed in a burn-in oven for heating the components **11**LF to a required temperature for a required time period.

The carrier **51**LF includes a base **120**LF; a cover **122**LF; an interconnect **52**LF; and a force applying member in the form of elastomeric spring members **124**LF. The base **120**LF and the cover **122**LF comprise an insulating material such as molded plastic or laminated ceramic, and are adapted for mating physical engagement. In addition, the base **120**LF and the cover **122**LF have a size that corresponds to the size of the leadframe substrate **10**LF. Clip members **128**LF removably secure the cover **122**LF to the base **120**LF with the leadframe substrate **10**LF therein. In addition, one or more vacuum openings **130**LF are formed in the cover **122**LF and in the spring member **124**LF, for securing the leadframe substrate **10**LF to the cover **122**LF during alignment and assembly of the leadframe test system **50**LF.

The base **120**LF includes an alignment member in the form of an alignment opening **138**LF having sloped side-

walls configured to engage the opposed longitudinal edges of the leadframe substrate **10**LF and to align the leadframe substrate **10**LF on the interconnect **52**LF. The base **120**LF also includes a recessed surface **140**LF configured to support the leadframe substrate **10**LF, and a cavity **142**LF wherein the interconnect **52**LF is mounted.

As shown schematically in FIG. **10**B, the interconnect **52**LF includes a pattern of interconnect contacts **54**LF. The size and shape of the alignment opening **138**LF, the recessed surface **140**LF, and the cavity **142**LF are such that the solder balls **43**LF on the leadframe substrate **10**LF align with the interconnect contacts **54**LF on the interconnect **52**LF. The interconnect contacts **54**LF are constructed as previously described for interconnect contacts **54**A (FIG. **5**B) and are adapted to form temporary electrical connections with the component contacts **43**LF on the components **11**LF.

The interconnect **52**LF also includes a switching network **56**LF (FIG. **10**A) in electrical communication with the interconnect contacts **54**LF. In this case the switching network **56**LF is contained on a separate die attached to the interconnect **52**LF. Conductors **73**LF on the interconnect **52**LF electrically connect the interconnect contacts **54**LF to the switching network **56**LF. In addition an electrical connector **132**LF such as a male or female edge connector is mounted to the interconnect **52**LF in electrical communication with the switching network **56**LF and the conductors **73**LF.

The leadframe test system **50**LF also includes a tester **62**LF having test circuitry **64**LF. In this case, the tester **62**LF can comprise a test board having a socket configured to electrically engage the electrical connector **132**LF.

Thus the invention provides an improved system and method for testing semiconductor components contained on a substrate. In each of the illustrative embodiments the switching network of the invention expands tester resources by multiplying write test signals from the tester to multiple semiconductor components. In addition, the switching network allows read test signals to be transmitted from multiple components up to the limit of tester resources. Further, the switching network can be used to electrically isolate selected components, such as defective components. The electrical isolation is particularly advantageous for burn in test procedures where "shared resources" are employed to test multiple components at the same time. The electrical isolation is also advantageous with interconnects that electrically engage multiple components at the same time, such as groups of components, or all of the components on a common substrate, such as a wafer.

While the invention has been described with reference to certain preferred embodiments, as will be apparent to those skilled in the art, certain changes and modifications can be made without departing from the scope of the invention as defined by the following claims.

What is claimed is:

1. A method for testing semiconductor components comprising:

providing a substrate containing the components;

providing an interconnect comprising a plurality of interconnect contacts configured to electrically engage the components;

providing a switching network in electrical communication with the interconnect contacts configured to control the interconnect contacts to selectively apply test signals to selected components, to electrically isolate defective components and to transmit read test signals from selected groups of components;

applying test signals through the switching network and the interconnect contacts to the components; and

controlling the test signals using the switching network to perform a selected test on the components.

2. The method of claim **1** wherein the interconnect electrically engages all of the components on the substrate at a same time.

3. The method of claim **1** wherein the selected test comprises functionality testing.

4. The method of claim **1** wherein the selected test comprises parametric testing.

5. The method of claim **1** wherein the selected test comprises burn-in testing.

6. The method of claim **1** wherein the substrate comprises a wafer, a panel, a leadframe or a module.

7. The method of claim **1** wherein the components comprise dice, packages or BGA devices.

8. A method for testing semiconductor components comprising:

providing a substrate containing the components and a plurality of component contacts on the components;

providing an interconnect comprising a plurality of interconnect contacts and a switching network in electrical communication with the interconnect contacts;

placing the component contacts and the interconnect contacts in physical and electrical contact;

transmitting test signals for performing functionality tests through the interconnect contacts to the components using the switching network to multiply and selectively transmit the test signals;

electrically isolating at least one non-functional component using the switching network;

transmitting write test signals for performing parametric testing through the interconnect contacts to selected components using the switching network to multiply and selectively transmit the write test signals; and

transmitting read test signals from selected groups of components using the switching network to group the components.

9. The method of claim **8** further comprising transmitting burn-in test signals to the components using the switching network to electrically isolate at least one defective components.

10. The method of claim **8** wherein the interconnect contacts electrically engage all of the component contacts on the substrate at a same time.

11. The method of claim **8** wherein the placing step is performed using a wafer prober.

12. The method of claim **8** wherein the placing step is performed using a carrier.

13. The method of claim **8** wherein the substrate comprises a wafer and the placing step is performed using a wafer prober.

14. The method of claim **8** wherein the substrate comprises a panel or a leadframe and the placing step is performed using a carrier.

15. A method for testing semiconductor components comprising:

providing a substrate containing the components;

providing a carrier configured to hold the substrate;

providing an interconnect on the carrier comprising a plurality of interconnect contacts configured to electrically engage the components;

providing a switching network on the interconnect configured to control the interconnect contacts to selectively apply test signals to the components;

applying test signals through the switching network and the interconnect contacts to the components; and

controlling the test signals using the switching network to perform a selected test on the components.

16. The method of claim **15** wherein the carrier comprises a base, a cover and a force applying mechanism.

17. The method of claim **15** wherein the carrier comprises an alignment member configured to align the substrate on the interconnect.

18. The method of claim **15** wherein the switching network is contained on a die attached to the interconnect.

19. The method of claim **15** wherein the interconnect comprises a semiconductor material and the switching network compress a plurality active electrical switching devices in the semiconductor material.

20. The method of claim **15** wherein the substrate comprises a panel and the components comprise semiconductor packages.

21. The method of claim **15** wherein the substrate comprises a leadframe and the components comprise semiconductor packages.

22. A method for testing semiconductor components comprising:

providing a substrate containing the components;

providing a carrier configured to hold the substrate;

providing a switching network on the carrier configured to control test signals to the components;

placing the substrate in the carrier;

performing a functionality test by applying functionality test signals through the switching network to the components; and

performing a burn-in test by applying burn-in test signals through the switching network to the components.

23. The method of claim **21** further comprising performing a parametric test by applying parametric test signals through the switching network to the components.

24. The method of claim **21** wherein the substrate comprises a wafer, a panel, a leadframe or a module substrate.

25. The method of claim **21** wherein the carrier comprises a base, a cover and a force applying mechanism.

26. The method of claim **21** wherein the carrier comprises an alignment member configured to align the substrate on the interconnect.

27. The method of claim **21** wherein the carrier comprises an interconnect and the switching network is on the interconnect.

28. A system for testing semiconductor components comprising:

a substrate containing the components;

an interconnect comprising a plurality of interconnect contacts configured to electrically engage all of the components on the substrate at a same time; and

a switching network in electrical communication with the interconnect contacts configured to selectively apply test signals to selected components, to electrically isolate defective components and to transmit read test signals from selected groups of components.

29. The system of claim **28** further comprising a carrier configured to hold the substrate and the interconnect.

30. The system of claim **28** wherein the substrate comprises a wafer, a panel, a leadframe or a module.

31. The system of claim **28** further comprising a tester in electrical communication with the interconnect contacts having tester resources expanded by the switching network.

32. The system of claim **28** further comprising a base for mounting the interconnect, a cover for holding the substrate, and a force applying mechanism for biasing the substrate and the interconnect together.

33. The system of claim **28** further comprising an alignment member configured to align the substrate on the interconnect.

34. A system for testing semiconductor components comprising:

a substrate containing the components;

a carrier configured to hold the substrate;

an interconnect on the carrier comprising a plurality of interconnect contacts configured to electrically engage the components; and

a switching network on the interconnect configured to control the interconnect contacts to selectively apply test signals to the components, to electrically isolate defective components and to transmit and to receive read test signals from selected groups of components.

35. The system of claim **34** wherein the carrier comprises a base wherein the interconnect is mounted and a force applying mechanism for biasing the substrate and the interconnect together.

36. The system of claim **34** wherein the carrier comprises an alignment member for aligning the substrate to the interconnect.

37. The system of claim **34** wherein the substrate comprises a wafer, a panel, a leadframe or a module.

38. The system of claim **34** wherein the interconnect is configured to electrically engage all of the components on the substrate at a same time.

39. The system of claim **34** wherein the substrate comprises a wafer and the components comprise semiconductor dice.

40. The system of claim **34** wherein the substrate comprises a panel and the components comprise semiconductor packages.

41. The system of claim **34** wherein the substrate comprises a leadframe and the components comprise semiconductor packages.

42. A system for testing semiconductor components comprising:

a substrate containing the components;

a testing apparatus configured to handle the substrate;

an interconnect on the testing apparatus comprising a plurality of interconnect contacts configured to electrically engage all of the components on the substrate at a same time;

a tester in electrical communication with the interconnect contacts configured to generate and analyze test signals and having tester resources determined by a signal generating and analyzing capability thereof; and

a switching network on the interconnect in electrical communication with the interconnect contacts configured to selectively apply the test signals to selected components, to electrically isolate defective components and to expand the tester resources by reading the test signals from selected groups of components.

43. The system of claim **42** wherein the testing apparatus comprises a wafer prober.

44. The system of claim **42** wherein the testing apparatus comprises a carrier configured to hold the substrate for burn-in testing.

45. The system of claim **42** wherein the testing apparatus comprises a base for holding the substrate and a force applying mechanism for biasing the substrate and the interconnect together.

46. The system of claim **42** wherein the testing apparatus comprises an alignment member configured to align the substrate to the interconnect.

47. The system of claim **42** wherein the interconnect comprises a plurality of interconnect contacts comprising conductive pockets or conductive projections.

48. A system for testing semiconductor components comprising:

a substrate containing the components;

a carrier configured to hold the substrate and to apply test signals to the components on the substrate, the carrier comprising an interconnect including a plurality of interconnect contacts configured to electrically engage the components, a force applying mechanism configured to bias the substrate and the interconnect together, and an alignment member configured to align the substrate on the interconnect; and

a switching network on the interconnect in electrical communication with the interconnect contacts configured to control the interconnect contacts and test signals to the components.

49. The system of claim **48** wherein the switching network comprises a die on the interconnect.

50. The system of claim **48** wherein the carrier comprises an electrical connector and the system further comprising a tester in electrical communication with the electrical connector.

51. The system of claim **48** wherein the system further comprises a tester and the switching network is configured to expand resources of the tester by transmitting read test signals from selected groups of components.

52. The system of claim **48** wherein the switching network comprises a plurality of active electrical switching devices.

53. The system of claim **48** wherein the substrate comprises a wafer and the components comprise dice on the wafer.

54. The system of claim **48** wherein the substrate compress a leadframe and the components comprise packages on the leadframe.

55. The system of claim **48** wherein the substrate comprises a panel and the components comprise packages on the panel.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,677,776 B2 Page 1 of 1
DATED : January 13, 2004
INVENTOR(S) : C. Patrick Doherty, Salman Akram and Jorge L. de Varona

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 13,
Line 12, change "compress" to -- comprises --

Signed and Sealed this

Twenty-fourth Day of February, 2004

Jon W. Dudas

JON W. DUDAS
Acting Director of the United States Patent and Trademark Office